

**United States Patent Application for:**

**CONTROLLING THE PROPERTIES AND UNIFORMITY  
OF A SILICON NITRIDE FILM BY CONTROLLING  
THE FILM FORMING PRECURSORS**

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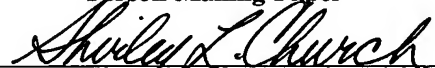
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1 [0001] CONTROLLING THE PROPERTIES AND UNIFORMITY OF A SILICON  
2 NITRIDE FILM BY CONTROLLING THE FILM FORMING PRECURSORS

3 [0002] **BACKGROUND OF THE INVENTION**

4 [0003] 1. Field of the Invention

5 [0004] The present invention pertains to a method of controlling the properties and  
6 uniformity of a silicon nitride film deposited by CVD (chemical vapor deposition) over a large  
7 surface area, and to the film produced by the method. In particular, the ion mobility and/or  
8 resistivity of the silicon nitride film are controlled within particular ranges.

9 [0005] 2. Brief Description of the Background Art

10 [0006] Current interest in thin film transistor (TFT) arrays is particularly high because  
11 these devices are used in liquid crystal active matrix displays of the kind often employed for  
12 computer and television flat panels. The liquid crystal active matrix displays may also  
13 contain light emitting diodes for back lighting. Further, organic light emitting diodes  
14 (OLEDs) have been used for active matrix displays, and these organic light emitting diodes  
15 require TFTs for addressing the activity of the displays.

16 [0007] The TFT arrays are typically created on a flat substrate. The substrate may be a  
17 semiconductor substrate, or may be a transparent substrate such as a glass, quartz, sapphire,  
18 or a clear plastic film. The TFT which is the subject of the present invention employs  
19 silicon-containing films, and in particular employs silicon nitride containing films for  
20 dielectric layers. A first silicon nitride-comprising film is referred to as the gate dielectric  
21 because it overlies the conductive gate electrode. A second silicon nitride-comprising film is  
22 referred to as the passivation dielectric and overlies the upper surface of a second conductive  
23 electrode, to electrically isolate the second conductive electrode from the ambient  
24 surrounding the upper surface of the TFT device (where the lower surface of the TFT device

1 is the glass, quartz, sapphire, plastic, or semiconductor substrate).

2 [0008] Figure 1 illustrates a schematic cross-sectional view of a thin film transistor  
3 structure of the kind which may employ both a silicon nitride-comprising gate dielectric film  
4 and a silicon nitride-comprising passivation dielectric film. This kind of thin film transistor  
5 is frequently referred to as an inverse staggered  $\alpha$ -Si TFT with a  $\text{SiN}_x$  layer as a gate  
6 insulator or as a back channel etch (BCE) inverted staggered (bottom gate) TFT structure.  
7 This structure is one of the more preferred TFT structures because the gate dielectric ( $\text{SiN}_x$ )  
8 and the intrinsic as well as n+ (or p+) doped amorphous silicon films can be deposited in a  
9 single PECVD pump-down run. The BCE TFT shown in Figure 1 involves only 4 or 5  
10 patterning masks.

11 [0009] As previously mentioned, the substrate 101 typically comprises a material that is  
12 essentially optically transparent in the visible spectrum, such as glass, quartz, sapphire, or a  
13 clear plastic. The substrate may be of varying shapes or dimensions. Typically, for TFT  
14 applications, the substrate is a glass substrate with a surface area greater than about  
15  $500 \text{ mm}^2$ . A gate electrode layer 102 is formed on the substrate 101. The gate electrode  
16 layer 102 may comprise a metal layer such as, for example, aluminum (Al), tungsten (W),  
17 chromium (Cr), tantalum (Ta), molybdenum (Mo), molybdenum tungsten (MoW), titanium  
18 (Ti), or combinations thereof, among others. The gate electrode layer 102 may be formed  
19 using conventional deposition, lithography and etching techniques. Between the substrate  
20 101 and the gate electrode layer 102, there may be an optional (not shown) insulating layer,  
21 for example, such a silicon oxide, or silicon nitride, which may also be formed using a  
22 PECVD system of the kind which will be described later herein.

23 [0010] A gate dielectric layer 103 is formed on the gate electrode layer 102. The gate  
24 dielectric layer may be silicon oxide, silicon oxynitride, or silicon nitride, deposited using  
25 such a PECVD system. The gate dielectric layer 103 may be formed to a thickness in the

1 range of about 100 Å to about 6,000 Å.

2 [0011] A bulk semiconductor layer 104 is formed on the gate dielectric layer 103. The  
3 bulk semiconductor layer 104 may comprise polycrystalline silicon (polysilicon),  
4 microcrystalline silicon ( $\mu\text{c-Si}$ ), or amorphous silicon ( $\alpha\text{-Si}$ ), which films can also be  
5 deposited using a PECVD system, or other conventional methods known in the art. Bulk  
6 semiconductor layer 104 may be deposited to a thickness in the range of about 100 Å to  
7 about 3,000 Å. A doped semiconductor layer 105 is formed on top of the semiconductor  
8 layer 104. The doped semiconductor layer 105 may comprise n-type (n+) or p-type (p+)  
9 doped polycrystalline, microcrystalline, or amorphous silicon. Doped semiconductor layer  
10 105 may be deposited to a thickness within a range of about 100 Å to about 3,000 Å. An  
11 example of the doped semiconductor layer 105 is n+ doped  $\alpha\text{-Si}$  film. The bulk  
12 semiconductor layer 104 and the doped semiconductor layer 105 are lithographically  
13 patterned and etched using conventional techniques to define a mesa of these two films over  
14 the gate dielectric insulator, which also serves as storage capacitor dielectric. The doped  
15 semiconductor layer 105 directly contacts portions of the bulk semiconductor layer 104,  
16 forming a semiconductor junction.

17 [0012] A conductive layer 106 is then deposited on the exposed surfaces of gate  
18 dielectric layer 103, semiconductor layer 104, and doped semiconductor layer 105. The  
19 conductive layer 106 may comprise a metal such as, for example, aluminum, tungsten,  
20 molybdenum, chromium, tantalum, and combinations thereof, among others. The  
21 conductive layer 106 may be formed using conventional deposition techniques. Both the  
22 conductive layer 106 and doped semiconductor layer 105 may be lithographically patterned  
23 to define source and drain contacts of the TFT, 106a and 106b, respectively in figure 1.  
24 After formation of the source and drain contacts 106a and 106b, a passivation dielectric  
25 layer 107 is typically applied. The passivation dielectric layer may be, for example, a silicon

1 oxide or a silicon nitride. The passivation layer 107 may be formed using, for example,  
2 PECVD or other conventional methods known in the art. The passivation layer 107 may be  
3 deposited to a thickness in the range of about 1,000Å to about 5,000 Å. The passivation  
4 layer 107 is then lithographically patterned and etched using conventional techniques, to  
5 open contact holes in the passivation layer.

6 [0013] A transparent electrically conductive layer 108 is then deposited and patterned to  
7 make contacts with the conductive layer 106. The transparent conductor layer 108  
8 comprises a material that is essentially optically transparent in the visible spectrum.  
9 Transparent conductor 108 may comprise, for example, indium tin oxide (ITO) or zinc oxide  
10 among others. Patterning of the transparent electrically conductive layer 108 is  
11 accomplished by conventional lithographic and etching methods.

12 [0014] There are a number of additional TFT structures which can employ silicon nitride  
13 gate insulators, and several of these are presented in a disclosure entitled "A Study on Laser  
14 Annealed Polycrystalline Silicon Thin Film Transistors (TFTs) with SiNx Gate Insulator",  
15 by Dr. Lee Kyung-ha (Kyung Hee University, 1998). This disclosure is available at  
16 <http://tftcd.khu.ac.kr/research/polySi>. Dr. Lee Kyung-ha's disclosure pertains mainly to the  
17 use of laser annealed poly-Si TFTs, which is not the subject matter of the present invention,  
18 but the TFT structures are of interest as background material. The structures of interest are  
19 presented in Chapter 2 of the disclosure.

20 [0015] D.B. Thomasson et al., in an article entitled: "High Mobility Tri-Layer a-Si:H  
21 Thin Film Transistors with Ultra-Thin Active Layer", 1977 Society for Information  
22 Display International Symposium Digest of Technical Papers, volume 28, pages 176 - 179,  
23 describe active matrix liquid crystal displays where the TFT has an active layer thickness of  
24 about 13 nm. The TFT structure is a glass substrate with a molybdenum bottom electrode, a  
25 silicon nitride gate dielectric layer, an a-Si:H layer overlying the silicon nitride gate

1 dielectric layer, n+  $\mu$ c-Si: H doped source and drain regions, separated by a silicon  
2 nitride dielectric mesa, and with an aluminum contact layer overlying each source and  
3 drain region. This is referred to as a Tri-layer a-Si:H TFT structure. The authors claim  
4 that such hydrogenated amorphous silicon thin-film transistors with active layer  
5 thickness of 13 nm perform better for display applications than devices with thicker (50  
6 nm) active layers. The linear ( $V_{DS} = 0.1$  V) and saturation region mobility of a 5  $\mu$ m  
7 channel length device is said to increase from 0.4  $\text{cm}^2/\text{V}\cdot\text{sec}$  and 0.7  $\text{cm}^2/\text{V}\cdot\text{sec}$  for a 50  
8 nm a-Si:H device to 0.7  $\text{cm}^2/\text{V}\cdot\text{sec}$  and 1.2  $\text{cm}^2/\text{V}\cdot\text{sec}$  for a 13 nm a-Si:H layer device  
9 fabricated with otherwise identical geometry and processing. The gate dielectric silicon  
10 nitride was deposited from a reactant gas mixture of  $\text{SiH}_4$ ,  $\text{NH}_3$ , and AR at 100  $\text{mW}/\text{cm}^2$ ,  
11 -150V, 0.5torr and 300 °C. The passivation silicon nitride dielectric layer was deposited  
12 at the same conditions as the gate dielectric, with the exception of substrate temperature,  
13 which was 250 °C.

14 [0016] Young-Bae Park et al., in an article entitled: "Bulk and interface properties of  
15 low-temperature silicon nitride films deposited by remote plasma enhanced chemical  
16 vapor deposition", Journal of Materials Science: Materials in Electronics 23 (2001) 515  
17 - 522, describe problems which occur when a gate dielectric, rather than being  $\text{SiN}_x$  is a  
18 hydrogenated silicon nitride film (a- $\text{SiN}_x$ :H). PECVD a- $\text{SiN}_x$ :H thin films are said to be  
19 widely used as a gate dielectric for a-Si:H TFT applications, due to the good interfacial  
20 property between an a-Si:H layer and an a-Si: $\text{N}_x$ : H layer. However, the a-Si :H TFTs  
21 with  $\text{SiN}_x$ :H gate dielectric is said to have instability problems such as the threshold  
22 voltage shift and the inverse subthreshold slope under a D.C. gate voltage bias. Their  
23 instability problems are said to be caused by the high trap density in the  $\text{SiN}_x$ : H film  
24 and the defects created at the a-Si : H/ $\text{SiN}_x$ :H interface. Charge trapping in the  $\text{SiN}_x$ :H  
25 is said to be from the electron injection under an applied field and due to the localized  
26 states of the Si dangling bonds, Si-H and N-H bonds in the forbidden gap. The authors  
27 claim that PECVD  $\text{SiN}_x$ :H dielectric films are not useful as a gate insulator because they

1 contain large amounts of bonded hydrogen (20 % - 40 %) in the form of N-H and Si-H  
2 bonds.

3 [0017] The authors propose that a remote plasma enhanced chemical vapor deposition  
4 of the gate dielectric layer be carried out. The  $\text{NH}_3$  precursor is excited in a remote  
5 plasma zone (at the top of the chamber) to produce  $\text{NH}^*$  or  $\text{NH}_2^* + \text{H}^*$ , after which the  
6 activated species\* from the plasma zone react with  $\text{SiH}_4$  introduced downstream through  
7 a gas dispersal ring to form the  $\text{SiN}_x\text{:H}$  electrical insulator with a reduction in the  
8 amounts of bonded hydrogen in the form of Si-H bonds, which are said to easily lose  
9 hydrogen to form a dangling bond of the kind known to reduce performance of the TFT  
10 device over time.

11 [0018] A presentation entitled: "Low Temperature a-Si:H TFT on Plastic Films:  
12 Materials and Fabrication Aspects", by Andrei Sazonov et al., Proc. 23rd International  
13 Conference on Microelectronics (MIEL 2002), Vol. 2, NIS, Yugoslavia, 12 - 15 May  
14 2002, related to fabrication technology for a-SiH thin film transistors at 120 °C for active  
15 matrix OLED displays on flexible plastic substrates. The TFTs produced were said to  
16 demonstrate performance very close to those fabricated at 260 °C. The authors claim  
17 that with the proper pixel integration, amorphous hydrogenated silicon (a-Si:H) TFTs are  
18 capable of supplying sufficiently high current to achieve required display brightness and  
19 thus can be a cost-effective solution for active matrix OLED displays.

20 [0019] The silicon nitride films used to produce the fabricated TFT samples were  
21 amorphous silicon nitride deposited at 120 °C by PECVD from  $\text{SiH}_4$  and  $\text{NH}_3$  gaseous  
22 precursors. The film is said to have a lower mass density and higher hydrogen  
23 concentration in comparison with films fabricated at 260 °C to 320 °C. In the study, a  
24 series of a-SiN<sub>x</sub>:H films with [N]/[Si] ratio ranging from 1.4 to 1.7 were deposited (at the  
25 120 °C). The hydrogen content in the films was in the range of 25 - 40 atomic percent.  
26 Generally, the films with higher [N]/[Si] are said to have higher mass density and higher  
27 compressive stress. The resistivity of a-SiN<sub>x</sub>:H films estimated at the field of 1MV/cm

1 was said to be in the range of  $10^{14}$  -  $10^{16}$  Ohm·cm, and the films with higher [N]/[Si]  
2 were said to have a higher breakdown field and dielectric constant than their lower N-  
3 content counterparts. A table of data supporting these conclusions is presented.

4 [0020] Compared to higher temperature counterparts, the lower temperature a-SiN<sub>x</sub>  
5 films are characterized by higher hydrogen content. The N-rich films with a hydrogen  
6 concentration of about 40 % or more exhibit hydrogen bonded predominantly to N  
7 atoms, with a high [N]/[Si] ratio achieved solely due to the high concentration of N-H  
8 bonds. The TFTs produced on a plastic film substrate at lower temperatures require a  
9 higher threshold voltage (4 - 5V) than the TFTs produced on glass at the higher  
10 temperatures. As a result, the ON current observed for TFTs produced at the lower  
11 temperatures is lower. Although the performance properties of these TFTs complies  
12 with the requirements for OLED applications, it is apparent that it would be beneficial to  
13 lower the threshold voltage of the TFTs produced at the 120 °C temperature.

14 [0021] As indicated above, the performance capabilities of the TFT are a direct result  
15 of the structural characteristics of the films formed during fabrication of the TFTs. The  
16 structural characteristics of the films depend directly upon the process conditions and  
17 relative amounts of precursors which are used during formation of the films which make  
18 up the TFTs. As the size of flat panel displays increase, it becomes increasingly difficult  
19 to control the uniformity of the individual films produced across the increased surface  
20 area. With respect to PECVD deposited silicon-nitride comprising films, which are used  
21 either as the gate dielectric layer or as the passivation dielectric layer, control of  
22 uniformity of the film across the substrate becomes particularly difficult when the  
23 PECVD is carried out in a process chamber having parallel-plate capacitively-coupled  
24 electrodes over about one meter by one meter. At the higher RF power applications, the  
25 RF power appears to concentrate at the center of the electrode area, resulting in a dome-  
26 shaped thickness profile, and film properties are indicative of the non-uniform power  
27 distribution across the electrodes. This kind of phenomena is more pronounced at the



1 higher RF power which is used to obtain film deposition rates (D/R) which are in excess  
2 of about 1000 Å/min.

3 [0022] Conventional PECVD processes for producing a-SiN<sub>x</sub>:H employ a precursor  
4 gas mixture which is highly diluted with nitrogen (N<sub>2</sub>) to obtain desired film properties.  
5 Such desired film properties are: a compressive film stress in the range of about 0 to  
6 - 10<sup>10</sup> dynes/cm<sup>2</sup>; low Si-H content of typically less than about 15 atomic %; and a low  
7 wet etch rate in HF solution (WER) of less than about 800 Å/min (normalized to thermal  
8 oxide at 1000 Å/min). However, a plasma produced at high concentrations of N<sub>2</sub> (where  
9 N<sub>2</sub> : SiH<sub>4</sub> is greater than 2 : 1) in the precursor gas, produces a particularly non-uniform  
10 plasma over a large surface area, for example a substrate having dimensions larger than  
11 about 1000 mm x 1000 mm (one square meter). This is believed to be due to the higher  
12 energy required to achieve dissociation of N<sub>2</sub> molecules. To overcome this problem with  
13 respect to the production of flat panel displays having large surface areas, the N<sub>2</sub>  
14 precursor gas was replaced by NH<sub>3</sub> precursor gas, which dissociates more easily.

15 [0023] More recently, there has been increased demand for even larger flat panel  
16 displays, for example those with substrates having dimensions larger than about 1500mm  
17 x 1800 mm. Initial efforts to produce flat panel displays of this size using a NH<sub>3</sub>  
18 precursor to supply nitrogen during formation of the a-SiN<sub>x</sub>:H gate dielectric films  
19 resulted in the formation of a-SiN<sub>x</sub>:H films exhibiting a higher hydrogen content in the  
20 film. As discussed above, this higher hydrogen content leads to a higher threshold  
21 voltage requirement for the TFT, which is harmful to performance of the TFT. There is  
22 presently a need for a process which permits formation of the a-SiN<sub>x</sub>:H gate dielectric  
23 films over large surface area substrates.

24 [0024] **SUMMARY OF THE INVENTION**

25 [0025] We have discovered and further developed a method of PECVD depositing an  
26 a-SiN<sub>x</sub>:H film useful as a TFT gate dielectric over surface areas larger than about 1000

1 mm x 1000 mm, where the uniformity of the film thickness and uniformity of film  
2 properties including chemical composition is surprisingly consistent. In particular, the  
3 film deposition rate is more than 1000 Å/min and typically more than 1300 Å/min; the  
4 Si-H bonded content of the a-SiN<sub>x</sub>:H film is less than about 15 atomic %; the film stress  
5 ranges from about 0 to about - 10<sup>10</sup> dynes/cm<sup>2</sup>; the film thickness across the substrate  
6 surface area varies by less than about 17 %; the refractive index (RI) of the film ranged  
7 from about 1.85 to about 1.95, and, the wet etch rate in HF solution (which is an  
8 indication of film density) is less than 800 Å/min. The HF solution is one referred to in  
9 the industry as "Buffer Oxide Etchant 6:1", which contains 7% by weight hydrofluoric  
10 acid, 34 % by weight ammonium fluoride, and 59 % by weight water. The wet etching  
11 test is carried out at a substrate temperature of about 25 °C. In addition, the chemical  
12 composition of the film, in terms of Si-H bonded content is consistently below the 15  
13 atomic % maximum preferred.

14 [0026] An a-SiN<sub>x</sub>:H gate dielectric film exhibiting the physical characteristics listed  
15 above provides excellent performance capabilities; and, the uniformity of the film across  
16 the substrate enables the production of flat panel displays having dimensions in the range  
17 of 1900 mm x 2200 mm, and possibly even larger.

18 [0027] In a previous effort to obtain a uniform distribution across a substrate having  
19 the dimensions of 1200 mm x 1300 mm, while providing an a-SiN<sub>x</sub>:H gate dielectric  
20 film exhibiting a low threshold voltage (low hydrogen content), we used precursor  
21 source gas (precursor gas mixture) having a NH<sub>3</sub>/SiH<sub>4</sub> ratio ranging from 3.1 to 8.6, a  
22 N<sub>2</sub>/SiH<sub>4</sub> ratio ranging from 10.0 to 35.8, and a N<sub>2</sub>/NH<sub>3</sub> ratio ranging from 2.4 to 10.0. A  
23 nitrogen content at this level did not cause a problem with film uniformity in terms of  
24 thickness and properties, including chemical composition across the substrate. However,  
25 we discovered that when the substrate size was increased to dimensions of 1500 mm to  
26 1800mm, this precursor source gas produced a nonuniform film thickness which varied  
27 by as much as about 25 %; produced film structures where the Si-H bonded content

1 exceeded 23 atomic %; and, produced films where the wet etch rate in HF solution  
2 (normalized to thermal oxide 1000 Å/min) exceeded 2400 Å/min in some instances.

3 Based on our earlier experience, the nitrogen content of the precursor source gas needed  
4 to be reduced to produce a more uniform film thickness across the substrate.

5 [0028] We were surprised to discover that by increasing the  $\text{NH}_3/\text{SiH}_4$  ratio to range  
6 between 5.3 to 10.0, while decreasing the  $\text{N}_2/\text{SiH}_4$  ratio to range between 5.5 and 18.7,  
7 and decreasing the spacing between electrodes by an amount between about 20 % and  
8 50 % from the baseline 1000 mils, we were able to deposit a-SiN<sub>x</sub>:H dielectric film with  
9 a film thickness which varied by less than about 16 % over the substrate surface, while  
10 maintaining a Si-H bonded content in the film of less than 15 atomic %. The  $\text{N}_2/\text{NH}_3$   
11 ratio which provided excellent results ranged from about 0.6 to about 2.5, preferably 0.6  
12 to about 2.3, which compared with the previous  $\text{N}_2/\text{NH}_3$  ratio of 2.4 to 10. We also  
13 maintained a wet etch rate below about 800 Å/min over the a-SiN<sub>x</sub>:H dielectric film  
14 surface using the new precursor source gas composition.

15 [0029] The critical requirement for deposition of an a-SiN<sub>x</sub>:H dielectric film used as  
16 a passivation layer is that the substrate temperature during deposition of the passivation  
17 layer is less than about 300 °C, to prevent damage to TFT channel ion migration  
18 characteristics and to reduce damage to the source/drain (S/D) metal as well. With this  
19 in mind, the passivation layer is deposited at a substrate temperature ranging between  
20 about 150 °C and about 300 °C, and preferably between about 260 °C and 280 °C. The  
21 general requirement in the industry for performance of the passivation layer is that the  
22 breakdown voltage not fall below about 5 MV/cm. The step coverage of the a-SiN<sub>x</sub>:H  
23 dielectric film used as a passivation layer needs to be better than for the gate dielectric  
24 film, to provide conformality over the S/D channel regions of the TFT device. The  
25 mechanical properties of the passivation layer are also important. For example, film  
26 stress for the passivation layer should be lower than for a gate dielectric layer. The film  
27 stress for the passivation layer should range between about  $+3 \times 10^{10}$  to about  $-3 \times 10^{10}$ .

1 Due to the decrease in deposition temperature, the wet etch rate of the deposited film  
2 typically increase (the density of the film decreases). One skilled in the art will need to  
3 balance the change in breakdown voltage, step coverage, and mechanical properties  
4 against other changes in device structure and properties to determine the best substrate  
5 temperature for deposition, based on the device performance requirements.

6 [0030] The combination process parameters required to produce the a-SiN<sub>x</sub>:H gate  
7 dielectric film having the properties and uniformity described above include the  
8 following:

9 A substrate temperature during film deposition which ranging from about  
10 120 °C to about 340 °C in general, and from about 320 °C to about 340 °C when the  
11 substrate is glass;

12 a process pressure of less than about 2.0 Torr, and typically ranges from about  
13 1.0 Torr to about 1.5 Torr;

14 a plasma density ranging between about 0.2 W/cm<sup>2</sup> and about 0.6 W/cm<sup>2</sup>;

15 a plasma precursor gas mixture in which the precursors gases include N<sub>2</sub>, NH<sub>3</sub>,  
16 and SiH<sub>4</sub>, and where the component ratios are NH<sub>3</sub>/SiH<sub>4</sub> ranging from about 5.3 to about  
17 10.0, N<sub>2</sub>/SiH<sub>4</sub> ranging from about 5.5 to about 18.7, and N<sub>2</sub>/NH<sub>3</sub> ranging from about 0.6  
18 to about 2.3, and typically from about 0.6 to about 1.9;

19 an electrode spacing in the PECVD process chamber which is appropriate for  
20 the substrate size and to meet film property requirements; and

21 a total precursor gas flow rate which is appropriate for the processing volume  
22 in the area of the substrate.

23 [0031] When the PECVD processing chamber is a parallel plate processing chamber,  
24 such as an AKT<sup>TM</sup> (Santa Clara, California) PECVD 25KA System (of the kind used to  
25 carry out the experimentation presented in the Examples herein), the electrode spacing  
26 should be less than about 1000 mils (a mil ≈ 0.001 inch), and typically ranges between  
27 about 800 and 400 mils. In addition, the total precursor gas flow rate should range from

1 about 20,000 sccm to about 70,000 sccm.

2 [0032] One skilled in the art can calculate an equivalent electrode spacing and  
3 precursor gas flow rate when the plasma processing chamber is different from the  
4 processing chamber specified above (and described in more detail subsequently herein).  
5 For example, substrates having surface areas up to 9 m<sup>2</sup> are contemplated.

6 [0033] The combination process parameters required to produce an a-SiN<sub>x</sub>:H  
7 passivation dielectric film are different from those required to produce a gate dielectric  
8 film. This is because the desired performance properties of the passivation dielectric  
9 layer are different, and because the device surface upon which the passivation dielectric  
10 layer is deposited is far more sensitive to substrate temperature at time of film deposition  
11 of the passivation dielectric layer. For example, the important performance  
12 characteristics of the passivation dielectric layer are not ion mobility and voltage  
13 threshold (as for the gate dielectric film), but are, instead, breakdown voltage, step  
14 coverage, and mechanical properties (such as residual film stress). An acceptable  
15 passivation layer may exhibit, for example, a WER of 5,000 or higher and a S-H bonded  
16 structure content of 20 % or higher and still be acceptable. With respect to the ratios of  
17 precursor gases used for PECVD of a passivation layer of a-SiN<sub>x</sub>:H, the ratio of  
18 NH<sub>3</sub>/SiH<sub>4</sub> may easily range, for example and not by way of limitation, from about 5.6 to  
19 about 11.1, typically from about 5.6 to about 10.6. The ratio of N<sub>2</sub>/SiH<sub>4</sub> may range, for  
20 example and not by way of limitation, from about 5.8 to about 20.8, and typically from  
21 about 5.8 to about 19.9. The ratio of N<sub>2</sub>/NH<sub>3</sub> may range, for example and not by way of  
22 limitation, from about 0.4 to about 2.3, and typically from about 0.6 to about 1.9.

23  
24 [0034] **BRIEF DESCRIPTION OF THE DRAWINGS**

25 [0035] Figure 1 shows a schematic cross-sectional view of one embodiment of a TFT  
26 device of the kind which employs the a-SiN<sub>x</sub>:H gate and passivation dielectric films of  
27 the present invention.

1 [0036] Figure 2 shows a PECVD processing chamber of the kind which can be used  
2 to deposit the films of the present invention.

3 [0037] Figure 3 shows a listing of all the steps which typically would be used to form  
4 a TFT structure of the kind shown in Figure 1, and provides a schematic top-view of a  
5 substrate including several TFT structures.

6 [0038] Figure 4A shows a graph illustrating the relationship between the atomic % of  
7 Si-H bonded structure in the a-SiN<sub>x</sub>:H dielectric film and the concentration of the Si-H  
8 bonded structure in terms of atoms which make up that structure/cm<sup>3</sup> of the a-SiN<sub>x</sub>:H  
9 dielectric film.

10 [0039] Figure 4B shows a graph which illustrates the relationship between the atomic  
11 % of the N-H bonded structure in the a-SiN<sub>x</sub>:H dielectric film and the concentration of  
12 the N-H bonded structure in terms of atoms which make up that structure/cm<sup>3</sup> of the a-  
13 SiN<sub>x</sub>:H dielectric film.

14 [0040] **DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS**

15 [0041] As a preface to the detailed description presented below, it should be noted  
16 that, as used in this specification and the appended claims, the singular forms "a", "an",  
17 and "the" include plural referents, unless the context clearly dictates otherwise.

18 [0042] We have developed a method of PECVD depositing a-SiN<sub>x</sub>:H films which are  
19 useful in a TFT device as gate dielectric and passivation layers, when a series of TFT  
20 devices are arrayed over a substrate having a surface area larger than about 1000 mm x  
21 1000 mm, which may be as large as 1900 mm x 2200 mm, and possibly even larger, up  
22 to a surface area of 9 m<sup>2</sup>, for example. The a-SiN<sub>x</sub>:H films provide a uniformity of film  
23 thickness and uniformity of film properties, including chemical composition, which are  
24 necessary independent of the substrate surface areas, but difficult to produce over large

1 surface areas.

2 [0043] We were surprised to discover that by increasing the  $\text{NH}_3/\text{SiH}_4$  ratio to range  
3 between 5.3 to 10.0, while decreasing the  $\text{N}_2/\text{SiH}_4$  ratio to range between 5.5 and 18.7,  
4 and decreasing the spacing between electrodes by an amount between about 20 % and 50  
5 % from the baseline 1000 mils, we were able to produce an  $\text{a-SiN}_x\text{:H}$  film which  
6 functioned well as a TFT gate dielectric. The film exhibited a thickness which varied by  
7 less than about 16 % over the substrate surface, while maintaining a Si-H bonded content  
8 in the film of less than 15 atomic %. We also maintained a wet etch rate of the  $\text{a-SiN}_x\text{:H}$   
9 deposited film below about 800 Å/min. The  $\text{N}_2/\text{NH}_3$  ratio which provided excellent  
10 results ranged from about 0.6 to about 2.5, preferably 0.6 to 2.3, which compared with  
11 the previous  $\text{N}_2/\text{NH}_3$  ratio of 2.4 to 10.

12 [0044] In addition to developing a method of producing an  $\text{a-SiN}_x\text{:H}$  dielectric film  
13 which functions well as a TFT gate dielectric, we developed an  $\text{a-SiN}_x\text{:H}$  dielectric film  
14 which functions well as a passivation layer overlying the upper conductive electrode of  
15 the TFT device. The critical requirement for deposition of an  $\text{a-SiN}_x\text{:H}$  passivation  
16 dielectric layer is that the substrate temperature during deposition is less than about  
17 300 °C (on a glass substrate), to prevent damage to TFT channel ion migration  
18 characteristics, and to reduce damage to the source/drain (S/D) metal as well. With this  
19 in mind, the passivation layer is deposited at a substrate temperature ranging between  
20 about 150 °C and about 300 °C, and preferably between about 260 °C and 280 °C. The  
21 general requirement for performance of the passivation layer is that the breakdown  
22 voltage not fall below about 5 MV/cm. The step coverage of the  $\text{a-SiN}_x\text{:H}$  dielectric  
23 passivation layer needs to be better than for the gate dielectric film, to provide  
24 conformality over the S/D channel regions of the TFT device. The mechanical properties  
25 of the passivation layer are also important. For example, the film stress for the  
26 passivation layer should range between about  $+3 \times 10^{10}$  to about  $-3 \times 10^{10}$ . Due to the  
27 decrease in deposition temperature, the wet etch rate of the deposited film typically

1 increase (the density of the film decreases). One skilled in the art will need to balance  
2 the change in breakdown voltage, step coverage, and mechanical properties against other  
3 changes in device structure and properties to determine the best substrate temperature for  
4 deposition, based on the device performance requirements.

5 [0045] I. AN APPARATUS FOR PRACTICING THE INVENTION

6 [0046] The embodiment example PECVD processes described herein were carried out  
7 in a parallel plate processing chamber, the AKT<sup>TM</sup> PECVD 25 KA System, available from  
8 AKT<sup>TM</sup>, a division of Applied Materials, Inc., Santa Clara, California. The system 200  
9 generally includes a processing chamber 202 coupled to a gas source 204. The processing  
10 chamber 202 has walls 206 and a bottom 208 that partially define a process volume 212.  
11 The process volume 212 is typically accessed through a port (not shown) in the walls 206  
12 that facilitate movement of a substrate 240 into and out of processing chamber 202. The  
13 walls 206 support a lid assembly 210 that contains a pumping plenum 214 that couples the  
14 process volume 212 to an exhaust port (that includes various pumping components, not  
15 shown).

16 [0047] A temperature controlled substrate support assembly 238 is centrally disposed  
17 within the processing chamber 202. The support assembly 238 supports the glass (for  
18 example, but not by way of limitation) substrate 240 during processing. The substrate  
19 support assembly 238 typically encapsulates at least one embedded heater 232, such as a  
20 resistive element, which element is coupled to an optional power source 230 and  
21 controllably heats the support assembly 238 and the substrate 240 positioned thereon.  
22 Typically, in a CVD process, the heater maintains the substrate 240 at a uniform temperature  
23 between about 120 °C and 460 °C, depending on the processing parameters of the substrate.

24 [0048] Generally, the support assembly 238 has a lower side 226 and an upper side 234.  
25 The upper side 234 supports the glass substrate 240. The lower side 226 has a stem 242  
26 coupled thereto. The stem 242 couples the support assembly 238 to a lift system (not



1 shown) that moves the support assembly 238 between an elevated processing position (as  
2 shown) and a lowered position that facilitates substrate transfer to and from the processing  
3 chamber 202. The stem 242 additionally provides a conduit for electrical and thermocouple  
4 leads between the support assembly 238 and other components of the system 200.

5 [0049] The support assembly 238 is generally grounded such that RF power supplied by  
6 a power source 222 to a gas distribution plate assembly 218 positioned between the lid  
7 assembly 210 and the substrate support assembly 238 (or other electrode positioned within  
8 or near the lid assembly of the chamber) may excite gases present in the process volume 212  
9 between the support assembly 238 and the distribution plate assembly 218. The RF power  
10 from the power source 222 is generally selected commensurate with the size of the substrate,  
11 to drive the chemical vapor deposition process. The distance "d" illustrates the spacing  
12 between the upper surface 230 of substrate support assembly 238 and the lower surface 231  
13 of distribution plate assembly 218. The spacing "d" in combination with the thickness of  
14 the substrate 240 substantially determines the processing volume 212. The spacing "d" can  
15 be adjusted as necessary to provide the desired processing conditions.

16 [0050] The lid assembly 210 typically includes an entry port 280 through which process  
17 gases provided by the gas source 204 are introduced into processing chamber 202. The entry  
18 port 280 is also coupled to a cleaning source 282. The cleaning source 282 typically  
19 provides a cleaning agent, such as disassociated fluorine, that is introduced into the  
20 processing chamber 202 to remove deposition by-products and films from processing  
21 chamber hardware.

22 [0051] The gas distribution plate assembly 218 is coupled to an interior side 220 of the  
23 lid assembly 210. The gas distribution plate assembly 218 is typically configured to  
24 substantially follow the profile of the substrate 230, for example, polygonal for large area  
25 substrates and circular for wafers. The gas distribution plate assembly 218 includes a  
26 perforated area 216 through which process and other gases supplied from the gas source 204  
27 are delivered to the process volume 212. The perforated area 216 of the gas distribution

1 plate assembly 218 is configured to provide uniform distribution of gases passing through  
2 the gas distribution plate assembly 218 into the processing chamber 202.

3 [0052] The gas distribution plate assembly 218 typically includes a diffuser plate 258  
4 suspended from a hanger plate 260. The diffuser plate 258 and hanger plate 260 may  
5 alternatively comprise a single unitary member. A plurality of gas passages 262 are formed  
6 through the diffuser plate 258 to allow a predetermined distribution of a precursor source  
7 gas passing through the gas distribution plate assembly 218 and into the process volume  
8 212. The hanger plate 260 maintains the diffuser plate 258 and the interior surface 220 of  
9 the lid assembly in a spaced-apart relation, thus defining a plenum 264 therebetween. The  
10 plenum 264 allows gases flowing through the lid assembly 210 to uniformly distribute  
11 across the width of the diffuser plate 258 so that gas is provided uniformly above the center  
12 perforated area 216 and flows with a uniform distribution through gas passages 262, passing

13 [0053] II. EXAMPLES

14 [0054] Example One, the Overall Process For Forming a TFT

15 [0055] To provide a general understanding of the relationship of the PECVD  
16 deposited a-SiN<sub>x</sub>:H gate dielectric film and the a-SiN<sub>x</sub>:H passivation dielectric film  
17 relative to the other components of the TFT, a brief description of the overall fabrication  
18 process of the TFT embodiment shown in Figure 1 is presented below.

19 [0056] Figure 3 show a series of process steps 300 which may be carried out to create  
20 the TFT device shown in Figure 1. Figure 3 also provides a schematic top-view 336 of a  
21 substrate including several TFT structures.

22 [0057] In the first step, "Gate Metal Sputtering", a conductive layer 302 is sputter  
23 deposited over a glass substrate 301 using techniques known in the art. In this particular  
24 instance the substrate 301 is a glass substrate having a thickness of 0.7 mm. The  
25 conductive layer 302 is actually a bilayer, where the bottom portion of the layer is a  
26 chrome layer, with an overlying layer of an aluminum neodymium alloy.

1 [0058] In the second step, "Gate Pattern (MASK 1)", the conductive layer 302 is  
2 pattern etched using a wet etch process known in the art to provide conductive electrodes  
3 302b.

4 [0059] In the third step, " $n^+$  a-Si / a-Si / a-SiN<sub>x</sub>:H PECVD", a layer 303 of a-SiN<sub>x</sub>:H  
5 is blanket applied by the PECVD process of the present invention, which is described in  
6 detail subsequently herein. Following the deposition of layer 303, a layer 304 of a-Si is  
7 blanket deposited using a PECVD process which is known in the art. Finally, a layer 305  
8 of  $n^+$  doped a-Si is blanket applied by processes known in the art, including a PECVD  
9 process, to provide a conductive layer which can later become the source and drain  
10 regions for the TFT device.

11 [0060] In the fourth step, "a-Si Pattern (MASK 2)", layers 304 of a-Si and 305 of  $n^+$   
12 doped a-Si are pattern dry etched, using techniques known in the art.

13 [0061] In the fifth step in the process, "S/D Sputtering", a blanket sputtering  
14 deposition of a chrome layer 306 is carried out using techniques known in the art. A  
15 portion of the chrome layer 306 subsequently becomes part of the source and drain  
16 regions of the TFT device.

17 [0062] In the sixth step, "S/D Pattern (MASK 3)", chrome layer 306 is pattern dry  
18 etched, using techniques known in the art.

19 [0063] In the seventh step in the process, " $n^+$  a-Si Etch-Back", the portion of the " $n^+$   
20 a-Si layer 305 which was exposed by the patterned dry etch in the sixth step is etched  
21 back using techniques known in the art. " $n^+$  a-Si layer 305 is etched completely through,  
22 and is "overetched" into underlying layer 304 of a-Si.

23 [0064] In the eighth step in the process, "SiN<sub>x</sub>:H PECVD", a passivation layer of a-  
24 SiN<sub>x</sub>:H dielectric 307 is applied over the substrate surface using PECVD, by the method  
25 of the present invention.

26 [0065] In the ninth process step, "Passivation Etch (MASK 4)", the passivation layer  
27 of a-SiN<sub>x</sub>:H dielectric 307 is pattern dry etched, using techniques known in the art.

1 [0066] In the tenth process step, "ITO Sputtering", a layer 308 of indium tin oxide is  
2 blanket sputter deposited over the substrate using techniques known in the art. The  
3 indium tin oxide layer 308 is a conductive optically clear layer when sputter deposited.  
4 This optically clear conductive layer enables the use of the TFT device for display  
5 applications.

6 [0067] In the eleventh process step, "ITO Pattern (MASK 5)", the indium tin oxide  
7 layer 308 is pattern dry etched using techniques known in the art to produce a patterned  
8 conductive layer which permits addressing of individual TFT structures which are shown  
9 in a schematic top view 336.

10 [0068] Example Two, the Process For Depositing an a-SiN<sub>x</sub>:H Gate Dielectric Layer

11 [0069] We have previously described all of the performance requirements for the a-  
12 SiN<sub>x</sub>:H gate dielectric layer. We carried out extensive experimentation in an effort to  
13 produce a PECVD deposited a-SiN<sub>x</sub>:H gate dielectric layer which met the performance  
14 requirements and which provided a uniformity in film thickness and uniformity in film  
15 properties, including structural and chemical composition, when PECVD deposited over  
16 a large surface area, larger than 1000 mm x 1000 mm, for example. One basic  
17 requirement is that the a-SiN<sub>x</sub>:H film deposition rate is more than 1000 Å/min and  
18 typically more than 1300 Å/min, so that the fabrication throughput for the TFT provides  
19 adequate productivity to be economically competitive. The basic requirements for the a-  
20 SiN<sub>x</sub>:H film are that: the Si-H bonded content of the a-SiN<sub>x</sub>:H film is less than about  
21 15 atomic %; the film stress ranges from about 0 to about - 10<sup>10</sup> dynes/cm<sup>2</sup>; the refractive  
22 index (RI) of the film ranges from about 1.85 to about 1.95, and, the wet etch rate in HF  
23 solution (Buffer Oxide Etchant 6 : 1), which WER is an indication of film density, is less  
24 than 800 Å/min. In addition, the chemical composition of the film, in terms of Si-H  
25 bonded content is consistently below the 15 atomic % maximum preferred. In an  
26 alternative embodiment structure to that shown in Figure 1, it is possible to deposit the a-  
27 SiN<sub>x</sub>:H gate dielectric layer at a high deposition rate initially (higher than about 1300

1 Å/min), where the Si-H bonded content may be as high as about 20 atomic % and then to  
2 deposit the a-SiN<sub>x</sub> : H gate dielectric layer at a low deposition rate (lower than about  
3 1300 Å/min, and typically lower than 1,000 Å/min), where the Si-H bonded content is  
4 below the 15 atomic % preferred maximum. This provides a good interface between the  
5 between the a-Si layer which is subsequently deposited over the a-SiN<sub>x</sub> : H gate dielectric  
6 layer. The film thickness uniformity across the substrate surface area should vary by less  
7 than about 17 %. With respect to uniformity of chemical composition of the film across  
8 the substrate, it is preferred that the S-H bonded structure not vary by more than 4 atomic  
9 %. With respect to uniformity of other film properties across the wafer, it is preferred  
10 that the variation in stress be less than about  $4 \times 10^9$  and that the wet etch rate (WER),  
11 which is also an indication of density, not vary more than 100 over the entire surface of  
12 the substrate.

13 [0070] Table 1 below presents data for experimental a-SiN<sub>x</sub> :H gate dielectric layer  
14 PECVD trials. This data is relative to physical properties of the a-SiN<sub>x</sub> :H gate  
15 dielectric layers produced. Table 2 below presents corresponding process parameter data  
16 for the experimental a-SiN<sub>x</sub> :H gate dielectric layer films which are described in Table 1.  
17 The "Run" numbers correspond. This process development was carried out in an AKT<sup>TM</sup>  
18 25 KA PECVD System of the kind previously described herein. Examples 1 - 6 are  
19 illustrative of deposited films which did not meet the target for the a-SiN<sub>x</sub> : H gate  
20 dielectric layer which is to interface with an overlying a-Si layer. Examples 7 - 11 are  
21 illustrative of films which did meet the target.

[0071] Table 1

[0072] Properties of the a-SiN<sub>x</sub>:H Gate Dielectric Film Deposited by PECVD

Run No.	Chamber Near Window Side "A"	Chamber Near Center "C"	Chamber Near Slit Valve Side "D"	Maximum Difference	D/R Å/min	Variation in Film Thickness Uniformity, % (excluding 15 mm from edge of substrate)
1					2015	13.2
Thick-ness Å	5991	5922	5895	96		
RI	1.89	1.89	1.87	0.02		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	+ 4.0	+ 1.8	+ 3.1	2.3		
N-H at %	16.6	16.5	16.9	0.4		
S-H at %	17.6	14.1	15.5	3.5		
WER Å/min	1575	960	1822	862		
2					2479	21.9
Thick-ness Å	6532	7970	6560	1438		
RI	1.90	1.91	1.90	0.01		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	+ 2.0	- 4.4	- 2.4	6.4		
N-H at %	18.6	22.5	23.2	4.6		
S-H at %	14.8	7.2	6.7	8.1		
WER Å/min	826	395	468	431		

\* + denotes tensile stress and - denotes compressive stress.

[0073] Table 1 Continued  
 [0074] Properties of the a-SiN<sub>x</sub>:H Gate Dielectric Film Deposited by PECVD

Run No.	Chamber Near Window Side "A"	Chamber Near Center "C"	Chamber Near Slit Valve Side "B"	Maximum Difference	D/R Å/min	Variation in Film Thickness Uniformity, % (excluding 15 mm from edge of substrate)
3					2364	10.8
Thick-ness Å	6605	7119	6641	514		
RI	1.88	1.89	1.87	0.02		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	+ 3.0	- 2.5	- 2.0	5.5		
N-H at %	21.6	26.1	27.5	5.9		
S-H at %	16.2	9.2	7.2	9.0		
WER Å/min	1137	554	882	583		
4					2653	9.6
Thick-ness Å	7830	7775	7271	559		
RI	1.91	1.93	1.92	0.02		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	+ 2.1	- 2.9	-0.5	5.0		
N-H at %	20.1	24.3	29.6	9.5		
S-H at %	23.0	19.6	26.9	7.3		
WER Å/min	784	363	664	421		

\* + denotes tensile stress and - denotes compressive stress.

[0075] Table 1 Continued

[0076] Properties of the a-SiN<sub>x</sub>:H Gate Dielectric Film Deposited by PECVD

Run No.	Chamber Near Window Side "A"	Chamber Near Center "C"	Chamber Near Slit Valve Side "B"	Maximum Difference	D/R Å/min	Variation in Film Thickness Uniformity, % (excluding 15 mm from edge of substrate)
<b>5</b>					2492	10.3
Thick-ness Å	7320	7929	7430	609		
RI	1.86	1.88	1.86	0.02		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	+ 4.4	- 1.1	+ 3.9	5.5		
N-H at %	19.2	23.2	24.8	5.6		
S-H at %	19.4	9.8	19.9	10.1		
WER Å/min	2422	821	2023	1601		
<b>6</b>					1374	15.7
Thick-ness Å	6165	7472	6086	1386		
RI	1.91	1.90	1.92	0.02		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	+ 2.5	- 1.6	+ 1.0	4.1		
N-H at %	17.5	21.1	18.0	3.6		
S-H at %	18.4	7.6	13.3	10.9		
WER Å/min	860	494	483	377		

\* + denotes tensile stress and - denotes compressive stress.



[0077] Table 1 Continued

[0078] Properties of the a-SiN<sub>x</sub>:H Gate Dielectric Film Deposited by PECVD

Run No.	Chamber Near Window Side "A"	Chamber Near Center "C"	Chamber Near Slit Valve Side "B"	Maximum Difference	D/R Å/min	Variation in Film Thickness Uniformity, % (excluding 15 mm from edge of substrate)
7					2286	16.2
Thick-ness Å	7013	8764	6999	1765		
RI	1.91	1.90	1.91	0.01		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	- 2.2	- 3.9	- 1.6	2.3		
N-H at %	20.5	20.7	20.7	0.2		
S-H at %	11.1	7.7	11.0	3.4		
WER Å/min	487	443	488	45		
8					1711	12.4
Thick-ness Å	6230	7413	6576	1183		
RI	1.91	1.90	1.90	0.01		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	- 1.0	- 3.7	-2.0	2.7		
N-H at %	22.5	24.5	22.9	2.0		
S-H at %	11.1	7.6	10.3	3.5		
WER Å/min	554	529	579	50		

\* + denotes tensile stress and - denotes compressive stress.

[0079]

Table 1 Continued

[0080] Properties of the a-SiN<sub>x</sub>:H Gate Dielectric Film Deposited by PECVD

Run No.	Chamber Near Window Side "A"	Chamber Near Center "C"	Chamber Near Slit Valve Side "B"	Maximum Difference	D/R Å/min	Variation in Film Thickness Uniformity, % (excluding 15 mm from edge of substrate)
9					1563	15.4
Thick-ness Å	5421	6758	5871	1337		
RI	1.92	1.91	1.91	0.01		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	- 5.3	- 8.1	- 5.3	2.8		
N-H at %	22.0	24.8	22.5	2.8		
S-H at %	7.8	4.8	7.9	3.1		
WER Å/min	381	404	410	29		
10					1622	13.3
Thick-ness Å	5555	6788	5857	1233		
RI	1.93	1.92	1.92	0.01		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	- 4.6	- 7.5	- 5.4	2.9		
N-H at %	22.6	25.3	23.8	2.7		
S-H at %	8.5	5.1	7.8	3.3		
WER Å/min	353	360	395	42		

\* + denotes tensile stress and - denotes compressive stress.

[0081] Table 1 Continued

[0082] Properties of the a-SiN<sub>x</sub>:H Gate Dielectric Film Deposited by PECVD

Run No.	Chamber Near Window Side "A"	Chamber Near Center "C"	Chamber Near Slit Valve Side "B"	Maximum Difference	D/R Å/min	Variation in Film Thickness Uniformity, % (excluding 15 mm from edge of substrate)
11					1327	8.3
Thick-ness Å	5888	6940	6131	1052		
RI	1.88	1.88	1.88	0.00		
Stress* x10 <sup>9</sup> dynes/cm <sup>2</sup>	- 2.3	- 4.2	- 2.1	2.1		
N-H at %	28.4	28.3	27.6	0.8		
S-H at %	4.7	2.9	4.7	1.8		
WER Å/min	739	695	767	72		

\* + denotes tensile stress and - denotes compressive stress.

[0083]

Table 2

[0084]

Process Conditions For Deposition of the a-SiN<sub>x</sub>:H Gate Dielectric Film  
Deposited by PECVD

Run No.	SiH <sub>4</sub> sccm	NH <sub>3</sub> sccm	N <sub>2</sub> sccm	RF <sup>1</sup> kW	Pr <sup>2</sup> Torr	Elect <sup>3</sup> Spcg Mil	DR <sup>4</sup> Å/min	NH <sub>3</sub> /SiH <sub>4</sub>	N <sub>2</sub> /SiH <sub>4</sub>	N <sub>2</sub> /NH <sub>3</sub>
1	2760	12340	30820	11	1.5	1090	2015	4.5	11.2	2.5
2	2800	9600	28000	15	1.5	1050	2479	3.4	10.0	2.9
3	2800	9600	28000	15	1.8	1050	2364	3.4	10.0	2.9
4	3500	12000	35000	15	1.5	1050	2653	3.4	10.0	2.9
5	3300	15600	38200	14.4	1.8	1050	2492	4.7	11.6	2.4
6	2000	8800	32000	9	1.4	1000	1374	4.4	16.0	3.6
7	3500	29000	22000	15	1.5	800	2286	8.3	6.3	0.8
8	2500	20000	22000	11	1.7	600	1711	8.0	8.8	1.1
9	3300	36000	18000	11	1.3	600	1563	10.6	5.5	0.5
10	3300	28000	18000	11	1.3	600	1622	8.5	5.5	0.5
11	1500	15000	28000	8	1.5	600	1327	10.0	18.7	1.9

1. RF power at 13.56 MHz.

2. Process chamber pressure.

3. Electrode spacing.

4. Deposition Rate.

[0085]

Conclusions based on the Examples:

[0086]

A review of all of the data presented herein indicates that it is possible to obtain an a-SiN<sub>x</sub>:H gate dielectric film useful as a TFT gate dielectric, where large numbers of the TFTs are arrayed over surface areas larger than about 1000 mm x 1000 mm. However, to obtain the uniformity of the film thickness and uniformity of film composition it is necessary to carefully control the process parameters used in production of the a-SiN<sub>x</sub>:H gate dielectric film. With respect to uniformity of chemical composition

1 of the film across the wafer, it is preferred that the S-H bonded structure not vary by  
2 more than 4 atomic %. With respect to uniformity of other film properties across the  
3 wafer, it is preferred that the variation in stress be less than about  $4 \times 10^9$  and that the wet  
4 etch rate (WER), which is also an indication of density, not vary more than 100 over the  
5 entire surface of the substrate.

6 [0087] As previously discussed, to meet industry requirements, it is preferred that the  
7 film deposition rate is more than 1000 Å/min and typically more than 1300 Å/min.  
8 Further, with respect to film properties of the a-SiN<sub>x</sub>:H gate dielectric film, the Si-H  
9 bonded content of the film should be less than about 15 atomic %; the film stress ranges  
10 from about 0 to about  $-10^{10}$  dynes/cm<sup>2</sup>; the film thickness across the substrate surface  
11 area varies by less than about 17 %; the refractive index (RI) of the film ranged from  
12 about 1.85 to about 1.95, and, the wet etch rate in HF solution (which is an indication of  
13 film density) is less than 800 Å/min. In addition, the chemical composition of the film,  
14 in terms of Si-H bonded content should be consistently below the 15 atomic %  
15 maximum limit.

16 [0088] An a-SiN<sub>x</sub>:H gate dielectric film exhibiting the physical characteristics listed  
17 above provides excellent performance capabilities; and, the uniformity of the film across  
18 the substrate enables the production of flat panel displays having dimensions in the range  
19 of 1870 mm x 2200 mm (a surface area of 4.1 m<sup>2</sup>), and even larger.

20 [0089] We were surprised to discover that by increasing the NH<sub>3</sub>/SiH<sub>4</sub> ratio to range  
21 between 5.3 to 10.0, while decreasing the N<sub>2</sub>/SiH<sub>4</sub> ratio to range between 5.5 and 18.7,  
22 we were able to deposit a-SiN<sub>x</sub>:H dielectric film with a film thickness which varied by  
23 less than about 16 % over the substrate surface, while maintaining a Si-H bonded content  
24 in the film of less than 15 atomic %. The resulting N<sub>2</sub>/NH<sub>3</sub> ratio due to this change  
25 ranged from about 0.6 to 1.9, which compared with the previous N<sub>2</sub>/NH<sub>3</sub> ratio of 2.4 to  
26 10. We also maintained a wet etch rate below about 800 Å/min over the a-SiN<sub>x</sub>:H  
27 dielectric film surface using the new precursor source gas composition.

1 [0090] The combination process parameters required to produce the a-SiN<sub>x</sub>:H gate  
2 dielectric film having the properties and uniformity described above include the  
3 following: A substrate temperature during film deposition which ranges from about 320  
4 °C to about 340 °C;

5 a process pressure of less than about 2.0 Torr, typically less than about 1.5  
6 Torr;

7 a plasma density ranging between about 0.2 W/cm<sup>2</sup> and about 0.6 W/cm<sup>2</sup>;

8 a plasma precursor gas mixture in which the precursors gases include N<sub>2</sub>, NH<sub>3</sub>,  
9 and SiH<sub>4</sub>, and where the component ratios are NH<sub>3</sub>/SiH<sub>4</sub> ranging from about 5.3 to about  
10 10.0, N<sub>2</sub>/SiH<sub>4</sub> ranging from about 5.5 to about 18.7, and N<sub>2</sub>/NH<sub>3</sub> ranging from about 0.6  
11 to about 2.3, typically from 0.6 to 1.9;

12 an electrode spacing in an AKT™ PECVD 25KA System, a parallel plate  
13 plasma processing chamber, which spacing is less than about 1000 mils (a mil - .001  
14 inch) and which typically ranges between about 800 mils and 400 mils;

15 and, a total precursor gas flow rate in the AKT™ PECVD 25KA System  
16 ranging from about 20,000 sccm to about 70,000 sccm.

17 [0091] One skilled in the art can calculate an equivalent electrode spacing and  
18 precursor gas flow rate when the plasma processing chamber is different from the  
19 processing chamber specified above (and described in more detail subsequently herein).

20 [0092] The combination process parameters required to produce an a-SiN<sub>x</sub>:H  
21 passivation dielectric film are different from those required to produce a gate dielectric  
22 film, as previously described in the Summary Of Invention. For example, the important  
23 performance characteristics of the passivation dielectric layer are not ion mobility and  
24 voltage threshold (as for the gate dielectric film), but are, instead, breakdown voltage,  
25 step coverage, and mechanical properties (such as residual film stress). An acceptable  
26 passivation layer may exhibit, for example, a WER of 5,000 or higher and a S-H bonded  
27 structure content of 20 % or higher and still be acceptable. With respect to the ratios of

precursor gases used for PECVD of a passivation layer of a-SiN<sub>x</sub>:H, the ratio of NH<sub>3</sub>/SiH<sub>4</sub> may easily range, for example and not by way of limitation, from about 5.6 to about 11.1, typically from about 5.6 to about 10.6. The ratio of N<sub>2</sub>/SiH<sub>4</sub> may range, for example and not by way of limitation, from about 5.8 to about 20.8, and typically from about 5.8 to about 19.9. The ratio of N<sub>2</sub>/NH<sub>3</sub> may range, for example and not by way of limitation, from about 0.4 to about 2.3, and typically from about 0.6 to about 1.9.

[0093] Figure 4A is a graph 410 which shows the relationship between the atomic weight % of Si-H bonded structure in the a-SiN<sub>x</sub>:H gate dielectric film and the concentration of the Si-H bonded structure in terms of atoms which make up that structure/cm<sup>3</sup> of the a-SiN<sub>x</sub>:H film. The atomic weight % of Si-H bonded structure is shown on the "x" axis which is labeled 412. The a-SiN<sub>x</sub>:H film density in atoms/cm<sup>3</sup> is shown on the "y" axis which is labeled 414. The relationship represented by curve 416 is  $y = 0.598 x$ , which is the correlation. This graph is presented for reference purposes to aid in understanding of the description of the invention.

[0094] Figure 4B is a graph 420 which shows the relationship between the atomic weight % of N-H bonded structure in the a-SiN<sub>x</sub>:H gate dielectric film and the concentration of the N-H bonded structure in terms of atoms which make up that structure/cm<sup>3</sup> of the a-SiN<sub>x</sub>:H film. The atomic weight % of N-H bonded structure is shown on the "x" axis which is labeled 422. The a-SiN<sub>x</sub>:H film density in atoms/cm<sup>3</sup> is shown on the "y" axis which is labeled 424. The relationship represented by curve 426 is  $y = 0.4443 x$ , which is the correlation. This graph is presented for reference purposes to aid in understanding of the description of the invention.

[0095] While the invention has been described in detail above with reference to several embodiments, various modifications within the scope and spirit of the invention will be apparent to those of working skill in this technological field. Accordingly, the scope of the invention should be measured by the appended claims.